## Features

- **80C52X2 Core (6 Clocks per Instruction)**
  - **Maximum Core Frequency 48 MHz in X1 Mode, 24MHz in X2 Mode**
  - **Dual Data Pointer**
  - **Full-duplex Enhanced UART (EUART)**
  - **Three 16-bit Timer/Counters: T0, T1 and T2**
  - **256 Bytes of Scratchpad RAM**
- **32-Kbyte On-chip Flash In-System Programming through USB or UART**
- **4-Kbyte EEPROM for Boot (3-Kbyte) and Data (1-Kbyte)**
- **On-chip Expanded RAM (ERAM): 1024 Bytes**
- **Integrated Power Monitor (POR/PFD) to Supervise Internal Power Supply**
- **USB 1.1 and 2.0 Full Speed Compliant Module with Interrupt on Transfer Completion**
  - **Endpoint 0 for Control Transfers: 32-byte FIFO**
  - **6 Programmable Endpoints with In or Out Directions and with Bulk, Interrupt or Isochronous Transfers**
    - **Endpoint 1, 2, 3: 32-byte FIFO**
    - **Endpoint 4, 5: 2 x 64-byte FIFO with Double Buffering (Ping-pong Mode)**
    - **Endpoint 6: 2 x 512-byte FIFO with Double Buffering (Ping-pong Mode)**
  - **Suspend/Resume Interrupts**
  - **Power-on Reset and USB Bus Reset**
  - **48 MHz DPLL for Full-speed Bus Operation**
  - **USB Bus Disconnection on Microcontroller Request**
- **5 Channels Programmable Counter Array (PCA) with 16-bit Counter, High-speed Output, Compare/Capture, PWM and Watchdog Timer Capabilities**
- **Programmable Hardware Watchdog Timer (One-time Enabled with Reset-out): 50 ms to 6s at 4 MHz**
- **Keyboard Interrupt Interface on Port P1 (8 Bits)**
- **TWI (Two Wire Interface) 400Kbit/s**
- **SPI Interface (Master/Slave Mode)**
- **34 I/O Pins**
- **4 Direct-drive LED Outputs with Programmable Current Sources: 2-6-10 mA Typical**
- **4-level Priority Interrupt System (11 sources)**
- **Idle and Power-down Modes**
- **0 to 32 MHz On-chip Oscillator with Analog PLL for 48 MHz Synthesis**
- **Industrial Temperature Range**
- **Low Voltage Range Supply: 3.0V to 3.6V**
- **Packages: SO28, MLF48, PLCC52, VQFP64**

Note: The AT89C5131A-L is the low voltage version of AT89C5131A-M, for functionnal information, please refer to AT89C5131A-M datasheet on the Atmel web site.

# 8-bit Flash Microcontroller with Full Speed USB Device

## AT89C5131A-L

## Preliminary

## Summary

Rev. 4338A–USB–08/04

Note: This is a summary document. A complete functional description is available in the AT89C5131A-M datasheet.

## Description

AT89C5131A-L is a high-performance Flash version of the 80C51 single-chip 8-bit microcontrollers with full speed USB functions.

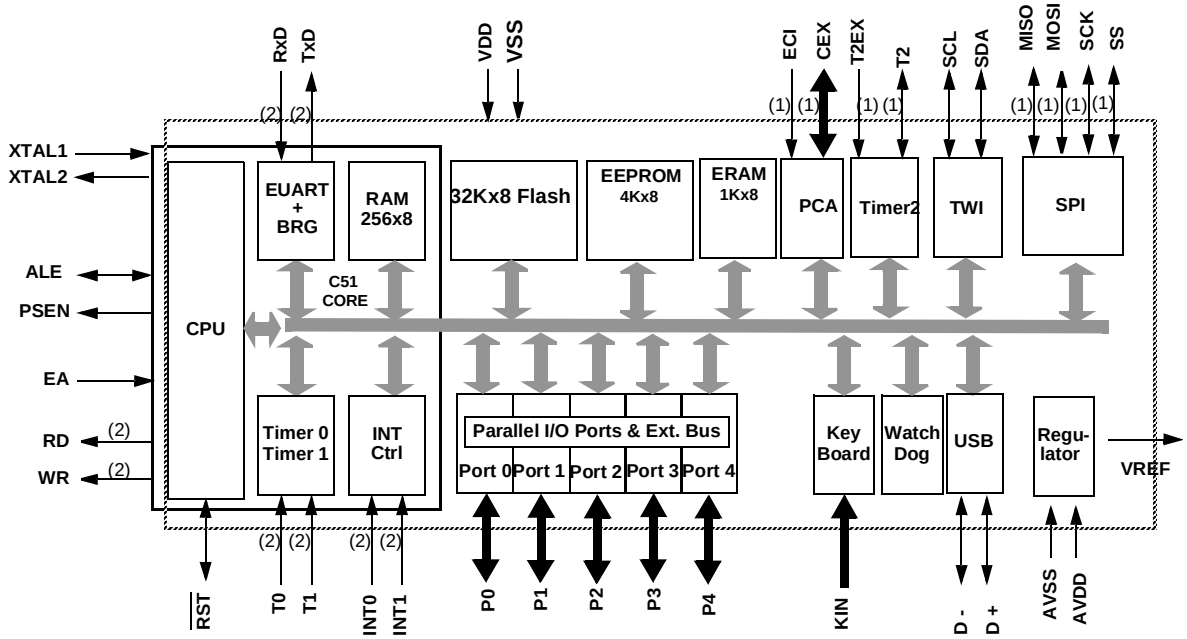
AT89C5131A-L features a full-speed USB module compatible with the USB specifications Version 1.1 and 2.0. This module integrates the USB transceivers with a 3.3V voltage regulator and the Serial Interface Engine (SIE) with Digital Phase Locked Loop and 48 MHz clock recovery. USB Event detection logic (Reset and Suspend/Resume) and FIFO buffers supporting the mandatory control Endpoint (EP0) and up to 6 versatile Endpoints (EP1/EP2/EP3/EP4/EP5/EP6) with minimum software overhead are also part of the USB module.

AT89C5131A-L retains the features of the Atmel 80C52 with extended Flash capacity (32-Kbyte), 256 bytes of internal RAM, a 4-level interrupt system, two 16-bit timer/counters (T0/T1), a full duplex enhanced UART (EUART) and an on-chip oscillator.

In addition, AT89C5131A-L has an on-chip expanded RAM of 1024 bytes (ERAM), a dual- data pointer, a 16-bit up/down Timer (T2), a Programmable Counter Array (PCA), up to 4 programmable LED current sources, a programmable hardware watchdog and a power-on reset.

AT89C5131A-L has two software-selectable modes of reduced activity for further reduction in power consumption. In the idle mode the CPU is frozen while the timers, the serial ports and the interrupt system are still operating. In the power-down mode the RAM is saved, the peripheral clock is frozen, but the device has full wake-up capability through USB events or external interrupts.

## Block Diagram




Notes: 1. Alternate function of Port 1
2. Alternate function of Port 3
3. Alternate function of Port 4

# Pinout Description

## Pinout

**Figure 1.** AT89C5131A-L 52-pin PLCC Pinout

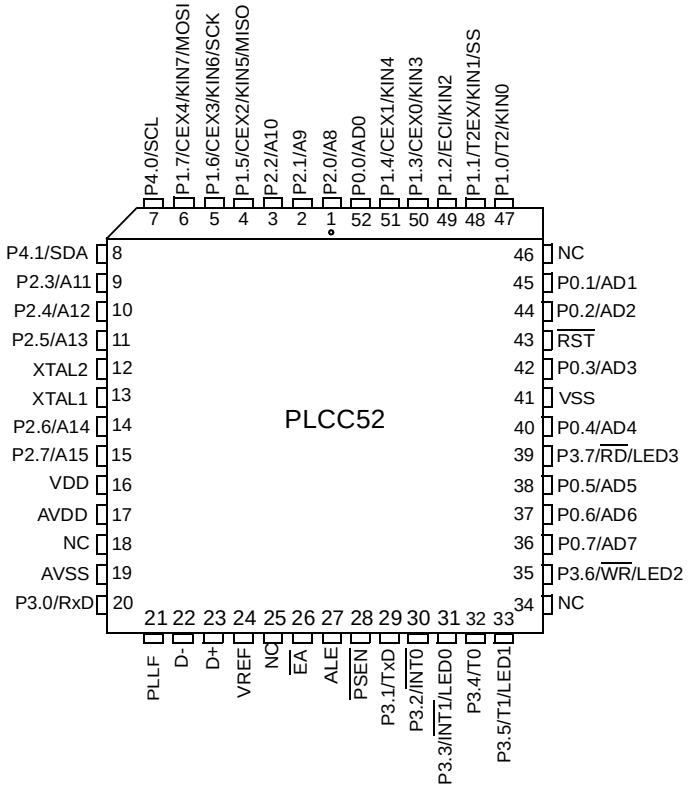


**Figure 2.** AT89C5131A-L 64-pin VQFP Pinout

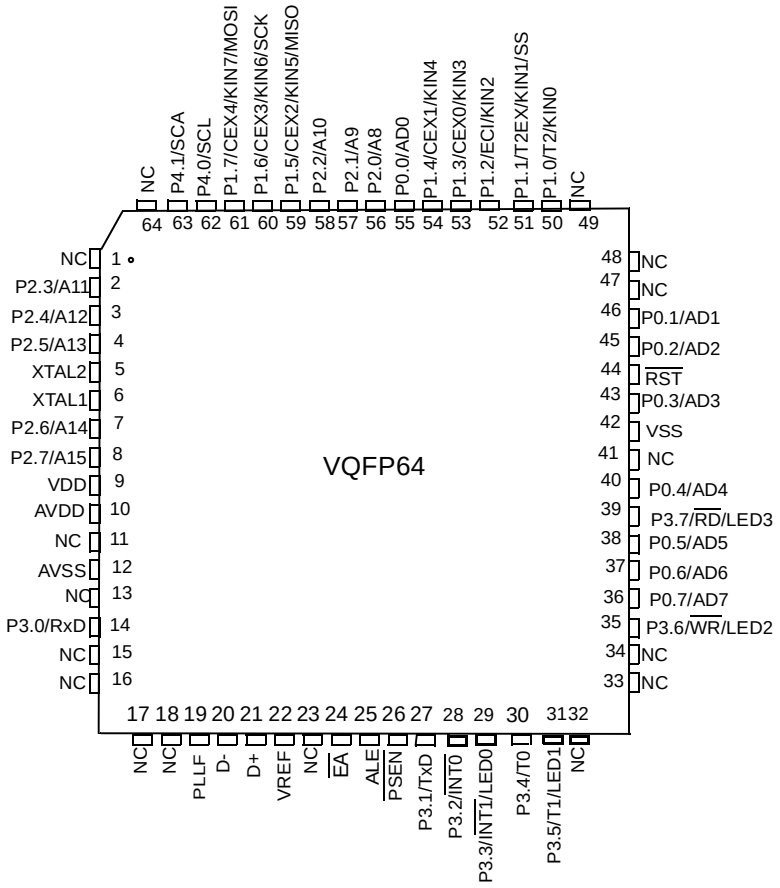
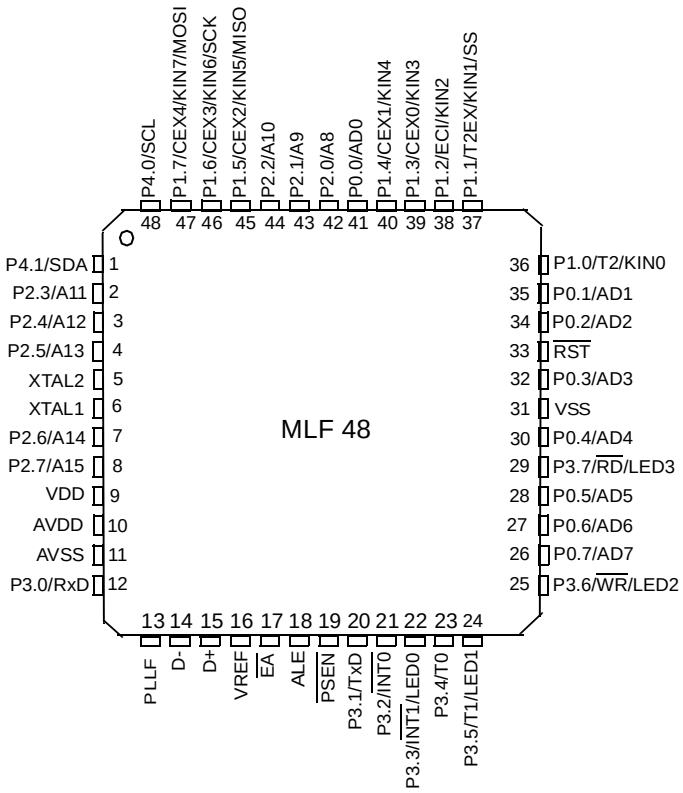


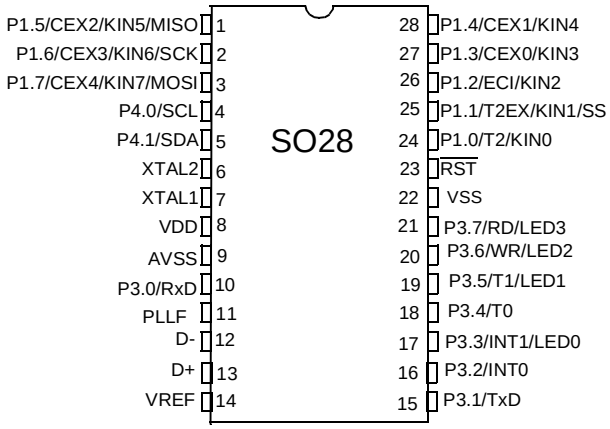
**Figure 3.** AT89C5131A-L 48-pin MLF Pinout




The MLF48 package does not allow external memory acces through P0/P2 ports (external code execution or external XRAM access).

P0 and P2 ports are output only ports for MLF48 package.

**Figure 4.** AT89C5131A-L 28-pin SO Pinout



## Signals

All the AT89C5131A-L signals are detailed by functionality on Table 1 through Table 12.

**Table 1.** Keypad Interface Signal Description

| Signal Name | Type | Description | Alternate Function |
|---|---|---|---|
| KIN[7:0] | I | **Keypad Input Lines**<br>Holding one of these pins high or low for 24 oscillator periods triggers a keypad interrupt if enabled. Held line is reported in the KBCON register. | P1[7:0] |

**Table 2.** Programmable Counter Array Signal Description

| Signal Name | Type | Description | Alternate Function |
|---|---|---|---|
| ECI | I | **External Clock Input** | P1.2 |
| CEX[4:0] | I/O | Capture External Input<br>Compare External Output | P1.3<br>P1.4<br>P1.5<br>P1.6<br>P1.7 |

**Table 3.** Serial I/O Signal Description

| Signal Name | Type | Description | Alternate Function |
|---|---|---|---|
| RxD | I | **Serial Input**<br>The serial input is P3.0 after reset, but it can also be configured to P4.0 by software. | P3.0 |
| TxD | O | **Serial Output**<br>The serial output is P3.1 after reset, but it can also be configured to P4.1 by software. | P3.1 |

**Table 4.** Timer 0, Timer 1 and Timer 2 Signal Description

| Signal Name | Type | Description | Alternate Function |
|---|---|---|---|
| INT0 | I | **Timer 0 Gate Input**<br>$\overline{INT0}$ serves as external run control for timer 0, when selected by GATE0 bit in TCON register.<br>**External Interrupt 0**<br>$\overline{INT0}$ input set IE0 in the TCON register. If bit IT0 in this register is set, bits IE0 are set by a falling edge on $\overline{INT0}$. If bit IT0 is cleared, bits IE0 is set by a low level on $\overline{INT0}$. | P3.2 |
| INT1 | I | **Timer 1 Gate Input**<br>$\overline{INT1}$ serves as external run control for Timer 1, when selected by GATE1 bit in TCON register.<br>**External Interrupt 1**<br>$\overline{INT1}$ input set IE1 in the TCON register. If bit IT1 in this register is set, bits IE1 are set by a falling edge on $\overline{INT1}$. If bit IT1 is cleared, bits IE1 is set by a low level on $\overline{INT1}$. | P3.3 |

**Table 4.** Timer 0, Timer 1 and Timer 2 Signal Description (Continued)

| Signal Name | Type | Description | Alternate Function |
|---|---|---|---|
| T0 | I | **Timer Counter 0 External Clock Input**<br>When Timer 0 operates as a counter, a falling edge on the T0 pin increments the count. | P3.4 |
| T1 | I | **Timer/Counter 1 External Clock Input**<br>When Timer 1 operates as a counter, a falling edge on the T1 pin increments the count. | P3.5 |
| T2 | I<br>O | **Timer/Counter 2 External Clock Input**<br>Timer/Counter 2 Clock Output | P1.0 |
| T2EX | I | Timer/Counter 2 Reload/Capture/Direction Control Input | P1.1 |

**Table 5.** LED Signal Description

| Signal Name | Type | Description | Alternate Function |
|---|---|---|---|
| LED[3:0] | O | **Direct Drive LED Output**<br>These pins can be directly connected to the Cathode of standard LEDs without external current limiting resistors. The typical current of each output can be programmed by software to 2, 6 or 10 mA. Several outputs can be connected together to get higher drive capabilities. | P3.3<br>P3.5<br>P3.6<br>P3.7 |

**Table 6.** TWI Signal Description

| Signal Name | Type | Description | Alternate Function |
|---|---|---|---|
| SCL | I/O | **SCL: TWI Serial Clock**<br>SCL output the serial clock to slave peripherals.<br>SCL input the serial clock from master. | P4.0 |
| SDA | I/O | **SDA: TWI Serial Data**<br>SCL is the bidirectional TWI data line. | P4.1 |

**Table 7.** SPI Signal Description

| Signal Name | Type | Description | Alternate Function |
|---|---|---|---|
| SS | I/O | **$\overline{\text{SS}}$:** SPI Slave Select | P1.1 |
| MISO | I/O | **MISO:** SPI Master Input Slave Output line<br>When SPI is in master mode, MISO receives data from the slave peripheral. When SPI is in slave mode, MISO outputs data to the master controller. | P1.5 |
| SCK | I/O | **SCK:** SPI Serial Clock<br>SCK outputs clock to the slave peripheral or receive clock from the master | P1.6 |
| MOSI | I/O | **MOSI:** SPI Master Output Slave Input line<br>When SPI is in master mode, MOSI outputs data to the slave peripheral. When SPI is in slave mode, MOSI receives data from the master controller | P1.7 |

**Table 8.** Ports Signal Description

| Signal Name | Type | Description | Alternate Function |
|---|---|---|---|
| P0[7:0] | I/O | **Port 0**<br>P0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. To avoid any parasitic current consumption, Floating P0 inputs must be pulled to $V_{DD}$ or $V_{SS}$. | AD[7:0] |
| P1[7:0] | I/O | **Port 1**<br>P1 is an 8-bit bidirectional I/O port with internal pull-ups, except for P1.6 and P1.7 that are true open drain outputs. | KIN[7:0]<br>T2<br>T2EX<br>ECI<br>CEX[4:0] |
| P2[7:0] | I/O | **Port 2**<br>P2 is an 8-bit bidirectional I/O port with internal pull-ups. | A[15:8] |
| P3[7:0] | I/O | **Port 3**<br>P3 is an 8-bit bidirectional I/O port with internal pull-ups. | LED[3:0]<br>RxD<br>TxD<br>$\overline{INT0}$<br>$\overline{INT1}$<br>T0<br>T1<br>$\overline{WR}$<br>$\overline{RD}$ |
| P4[1:0] | I/O | **Port 4**<br>P4 is an 2-bit open port. | SCL<br>SDA |

**Table 9.** Clock Signal Description

| Signal Name | Type | Description | Alternate Function |
|---|---|---|---|
| XTAL1 | I | **Input to the on-chip inverting oscillator amplifier**<br>To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, its output is connected to this pin. | - |
| XTAL2 | O | **Output of the on-chip inverting oscillator amplifier**<br>To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, leave XTAL2 unconnected. | - |
| PLLF | I | **PLL Low Pass Filter input**<br>Receives the RC network of the PLL low pass filter (See Figure 5 on page 13 ). | - |

**Table 10.** USB Signal Description

| Signal Name | Type | Description | Alternate Function |
|---|---|---|---|
| D+ | I/O | USB Data + signal | - |
| D- | I/O | USB Data - signal | - |
| VREF | O | **USB Reference Voltage**<br>Connect this pin to D+ using a 1.5 kΩ resistor to use the Detach function. | - |

**Table 11.** System Signal Description

| Signal Name | Type | Description | Alternate Function |
|---|---|---|---|
| AD[7:0] | I/O | Multiplexed Address/Data LSB for external access<br>Data LSB for Slave port access (used for 8-bit and 16-bit modes) | P0[7:0] |
| A[15:8] | I/O | Address Bus MSB for external access<br>Data MSB for Slave port access (used for 16-bit mode only) | P2[7:0] |
| RD | I/O | **Read Signal**<br>Read signal asserted during external data memory read operation.<br>Control input for slave port read access cycles. | P3.7 |
| WR | I/O | **Write Signal**<br>Write signal asserted during external data memory write operation.<br>Control input for slave write access cycles. | P3.6 |
| $\overline{RST}$ | I/O | **Reset**<br>Holding this pin low for 64 oscillator periods while the oscillator is running resets the device. The Port pins are driven to their reset conditions when a voltage lower than $V_{IL}$ is applied, whether or not the oscillator is running. This pin has an internal pull-up resistor which allows the device to be reset by connecting a capacitor between this pin and VSS.<br>Asserting $\overline{RST}$ when the chip is in Idle mode or Power-down mode returns the chip to normal operation.<br>This pin is set to 0 for at least 12 oscillator periods when an internal reset occurs (hardware watchdog or Power monitor). | - |
| ALE | O | **Address Latch Enable Output**<br>The falling edge of ALE strobes the address into external latch. This signal is active only when reading or writing external memory using MOVX instructions. | - |
| PSEN | O | **Program**<br>Test mode entry signal. This pin must be set to $V_{DD}$ for normal operation. | - |
| EA | I | **External Access Enable**<br>This pin must be held low to force the device to fetch code from external program memory starting at address 0000h. It is latched during reset and cannot be dynamically changed during operation. | - |

**Table 12.** Power Signal Description

| Signal Name | Type | Description | Alternate Function |
|---|---|---|---|
| AVSS | GND | **Alternate Ground**<br>AVSS is used to supply the on-chip PLL and the USB PAD. | - |
| AVDD | PWR | **Alternate Supply Voltage**<br>AVDD is used to supply the on-chip PLL and the USB PAD. | - |
| VSS | GND | **Digital Ground**<br>VSS is used to supply the buffer ring and the digital core. | - |
| VDD | PWR | **Digital Supply Voltage**<br>VDD is used to supply the buffer ring on all versions of the device.<br>It is also used to power the on-chip voltage regulator of the Standard versions or the digital core of the Low Power versions. | - |

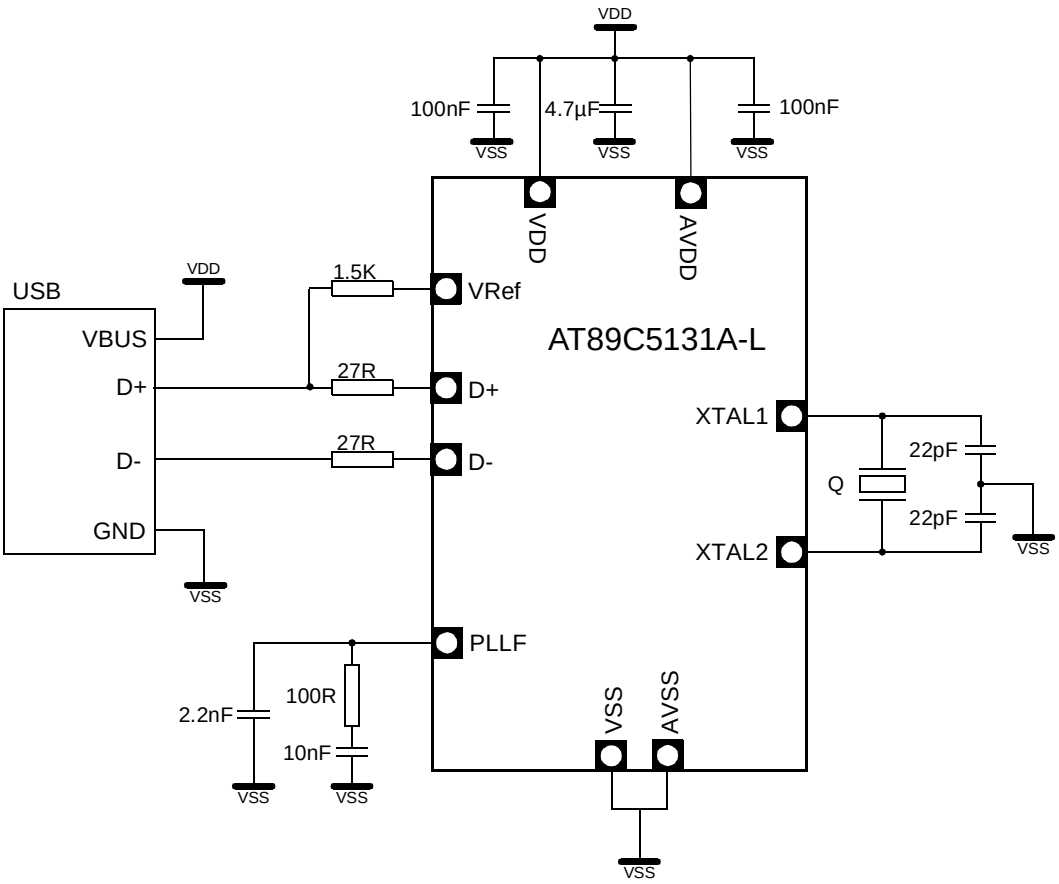
**Table 12.** Power Signal Description (Continued)

| Signal Name | Type | Description | Alternate Function |
|---|---|---|---|
| VREF | O | **USB pull-up Controlled Output**<br>VREF is used to control the USB D+ 1.5 kΩ pull up.<br>The Vref output is in high impedance when the bit DETACH is set in the USBCON register. | - |

## Typical Application

The following figure represents the typical wiring schematic.

**Figure 5.** Typical Application



# Electrical Characteristics

## Absolute Maximum Ratings

Ambient Temperature Under Bias:

I = industrial .....-40°C to 85°C

Storage Temperature ..... -65°C to + 150°C

Voltage on $V_{CC}$ from $V_{SS}$.....-0.5V to + 6V

Voltage on Any Pin from $V_{SS}$ .....-0.5V to $V_{CC}$ + 0.2V

Note: Stresses at or above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

## DC Parameters

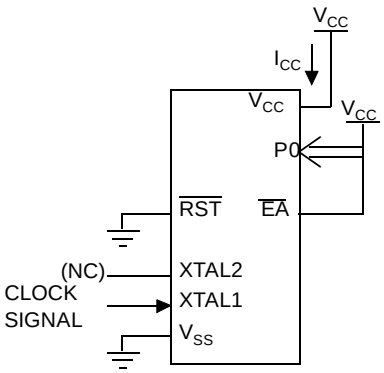
$T_A$ = -40°C to +85°C; $V_{SS}$ = 0V; $V_{CC}$ = 3.3V ± 10%; F = 0 to 40 MHz

| Symbol | Parameter | Min | Typ[5] | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | -0.5 | | 0.2Vcc - 0.1 | V | |
| $V_{IH}$ | Input High Voltage except XTAL1, $\overline{RST}$ | 0.2 $V_{CC}$ + 0.9 | | $V_{CC}$ + 0.5 | V | |
| $V_{IH1}$ | Input High Voltage, XTAL1, $\overline{RST}$ | 0.7 $V_{CC}$ | | $V_{CC}$ + 0.5 | V | |
| $V_{OL}$ | Output Low Voltage, ports 1, 2, 3 and 4[6] | | | 0.3<br>0.45<br>1.0 | V<br>V<br>V | $I_{OL}$ = 100 µA[4]<br>$I_{OL}$ = 0.8 mA[4]<br>$I_{OL}$ = 1.6mA[4] |
| $V_{OL1}$ | Output Low Voltage, port 0, ALE, $\overline{PSEN}$ [6] | | | 0.3<br>0.45<br>1.0 | V<br>V<br>V | $I_{OL}$ = 200 µA[4]<br>$I_{OL}$ = 1.6 mA[4]<br>$I_{OL}$ = 3.5 mA[4] |
| $V_{OH}$ | Output High Voltage, ports 1, 2, 3, 4 and 5 | $V_{CC}$ - 0.3<br>$V_{CC}$ - 0.7<br>$V_{CC}$ - 1.5 | | | V<br>V<br>V | $I_{OH}$ = -10 µA<br>$I_{OH}$ = -30 µA<br>$I_{OH}$ = -60 µA<br>$V_{CC}$ = 3.3V ± 10% |
| $V_{OH1}$ | Output High Voltage, port 0, ALE, $\overline{PSEN}$ | $V_{CC}$ - 0.3<br>$V_{CC}$ - 0.7<br>$V_{CC}$ - 1.5 | | | V<br>V<br>V | $I_{OH}$ = -200 µA<br>$I_{OH}$ = -1.6 mA<br>$I_{OH}$ = -3.5 mA<br>$V_{CC}$ = 3.3V ± 10% |
| $R_{RST}$ | $\overline{RST}$ Pullup Resistor | 50 | 100 | 200 | kΩ | |
| $I_{IL}$ | Logical 0 Input Current ports 1, 2, 3 and 4 | | | -50 | µA | Vin = 0.45V |
| $I_{LI}$ | Input Leakage Current | | | ±10 | µA | 0.45V < Vin < $V_{CC}$ |
| $I_{TL}$ | Logical 1 to 0 Transition Current, ports 1, 2, 3 and 4 | | | -650 | µA | Vin = 2.0V |
| $C_{IO}$ | Capacitance of I/O Buffer | | | 10 | pF | Fc = 1 MHz<br>$T_A$ = 25°C |
| $I_{PD}$ | Power-down Current | | TBD | | µA | 3.0V < $V_{CC}$ < 3.6V[3] |
| $I_{CC}$ | Power Supply Current | $I_{CCOP}$ = TBD mA<br>$I_{CCIDLE}$ = TBD mA | | | | $V_{CC}$ = 3.3V [1][2] |
| $V_{PFDP}$ | Power Fail High Level Threshold | | | 3.0 | V | |

| Symbol | Parameter | Min | Typ[5] | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{PFDM}$ | Power Fail Low Level Threshold | 2.2 | | | V | |
| | Power fail hysteresis $V_{PFDP}$ - $V_{PFDM}$ | 0.15 | | | V | |

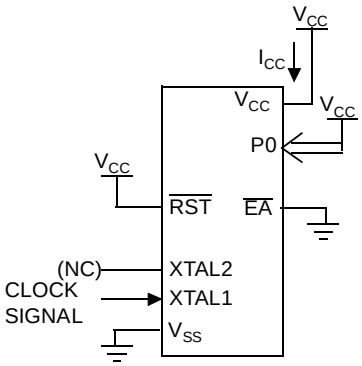
Notes:
1. Operating $I_{CC}$ is measured with all output pins disconnected; XTAL1 driven with $T_{CLCH}$, $T_{CHCL}$ = 5 ns (see Figure 9.), $V_{IL}$ = $V_{SS}$ + 0.5V, $V_{IH}$ = $V_{CC}$ - 0.5V; XTAL2 N.C.; $\overline{EA}$ = $\overline{RST}$ = Port 0 = $V_{CC}$. $I_{CC}$ would be slightly higher if a crystal oscillator used (see Figure 6.).
2. Idle $I_{CC}$ is measured with all output pins disconnected; XTAL1 driven with $T_{CLCH}$, $T_{CHCL}$ = 5 ns, $V_{IL}$ = $V_{SS}$ + 0.5V, $V_{IH}$ = $V_{CC}$ - 0.5V; XTAL2 N.C; Port 0 = $V_{CC}$; $\overline{EA}$ = $\overline{RST}$ = $V_{SS}$ (see Figure 7).
3. Power-down $I_{CC}$ is measured with all output pins disconnected; $\overline{EA}$ = $V_{CC}$, PORT 0 = $V_{CC}$; XTAL2 NC.; $\overline{RST}$ = $V_{SS}$ (see Figure 8.). In addition, the WDT must be inactive and the POF flag must be set.
4. Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the $V_{OLS}$ of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operation. In the worst cases (capacitive loading 100 pF), the noise pulse on the ALE line may exceed 0.45V with maxi $V_{OL}$ peak 0.6V. A Schmitt Trigger use is not necessary.
5. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature.
6. Under steady state (non-transient) conditions, $I_{OL}$ must be externally limited as follows:
   Maximum $I_{OL}$ per port pin: 10 mA
   Maximum $I_{OL}$ per 8-bit port:
   Port 0: 26 mA
   Ports 1, 2 and 3: 15 mA
   Maximum total $I_{OL}$ for all output pins: 71 mA
   If $I_{OL}$ exceeds the test condition, $V_{OL}$ may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

**Figure 6.** $I_{CC}$ Test Condition, Active Mode



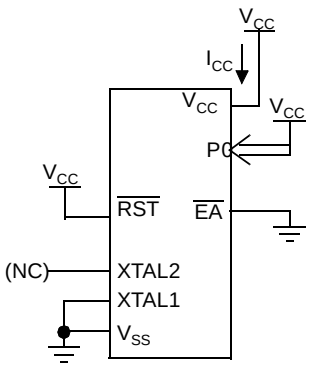

All other pins are disconnected.

**Figure 7.** $I_{CC}$ Test Condition, Idle Mode



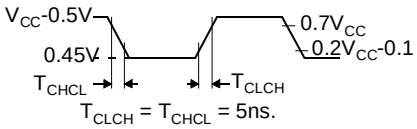

All other pins are disconnected.

**Figure 8.** $I_{CC}$ Test Condition, Power-down Mode




All other pins are disconnected.

**Figure 9.** Clock Signal Waveform for $I_{CC}$ Tests in Active and Idle Modes



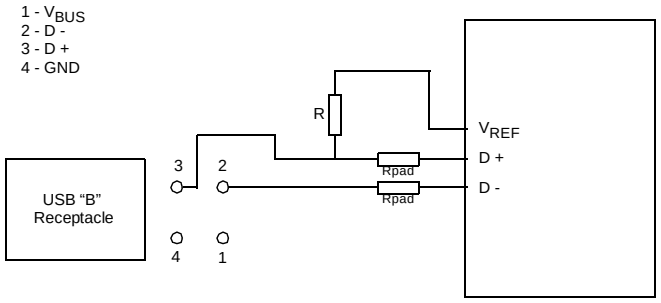

**LED's**

**Table 13.** LED Outputs DC Parameters

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $I_{OL}$ | Output Low Current, P3.6 and P3.7 LED modes | 1 | 2 | 4 | mA | 2 mA configuration |
| | | 2 | 4 | 8 | mA | 4 mA configuration |
| | | 5 | 10 | 20 | mA | 10 mA configuration |

Note: 1. ($T_A$ = -20°C to +50°C, $V_{CC}$ - $V_{OL}$ = 2 V ± 20%)

## USB DC Parameters




R = 1.5 kΩ
$R_{pad}$ = 27Ω

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{REF}$ | USB Reference Voltage | 3.0 | | 3.6 | V |
| $V_{IH}$ | Input High Voltage for D+ and D- (Driven) | 2.0 | | | V |
| $V_{IHZ}$ | Input High Voltage for D+ and D- (Floating) | 2.7 | | 3.6 | V |
| $V_{IL}$ | Input Low Voltage for D+ and D- | | | 0.8 | V |
| $V_{OH}$ | Output High Voltage for D+ and D- | 2.8 | | 3.6 | V |
| $V_{OL}$ | Output Low Voltage for D+ and D- | 0.0 | | 0.3 | V |

## AC Parameters

### Explanation of the AC Symbols

Each timing symbol has 5 characters. The first character is always a “T” (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

Example: $T_{AVLL}$ = Time for Address Valid to ALE Low.
$T_{LLPL}$ = Time for ALE Low to $\overline{PSEN}$ Low.

$T_A$ = -40°C to +85°C; $V_{SS}$ = 0V; $V_{CC}$ = 3.3V ±10%; F = 0 to 40 MHz.

$T_A$ = -40°C to +85°C; $V_{SS}$ = 0V; $V_{CC}$ = 3.3V ± 10%.

(Load Capacitance for port 0, ALE and PSEN = 60 pF; Load Capacitance for all other outputs = 60 pF.)

Table 14, Table 17 and Table 20 give the description of each AC symbols.

Table 15, Table 19 and Table 21 give for each range the AC parameter.

Table 16, Table 19 and Table 22 give the frequency derating formula of the AC parameter for each speed range description. To calculate each AC symbols. take the x value and use this value in the formula.

Example: $T_{LLIV}$ and 20 MHz, Standard clock.
x = 30 ns
T = 50 ns
$T_{CCIV}$ = 4T - x = 170 ns

### External Program Memory Characteristics

**Table 14.** Symbol Description

| Symbol | Parameter |
|---|---|
| T | Oscillator Clock Period |
| $T_{LHLL}$ | ALE Pulse Width |
| $T_{AVLL}$ | Address Valid to ALE |
| $T_{LLAX}$ | Address Hold after ALE |
| $T_{LLIV}$ | ALE to Valid Instruction In |
| $T_{LLPL}$ | ALE to $\overline{PSEN}$ |
| $T_{PLPH}$ | $\overline{PSEN}$ Pulse Width |
| $T_{PLIV}$ | $\overline{PSEN}$ to Valid Instruction In |
| $T_{PXIX}$ | Input Instruction Hold after $\overline{PSEN}$ |
| $T_{PXIZ}$ | Input Instruction Float after $\overline{PSEN}$ |
| $T_{AVIV}$ | Address to Valid Instruction In |
| $T_{PLAZ}$ | $\overline{PSEN}$ Low to Address Float |

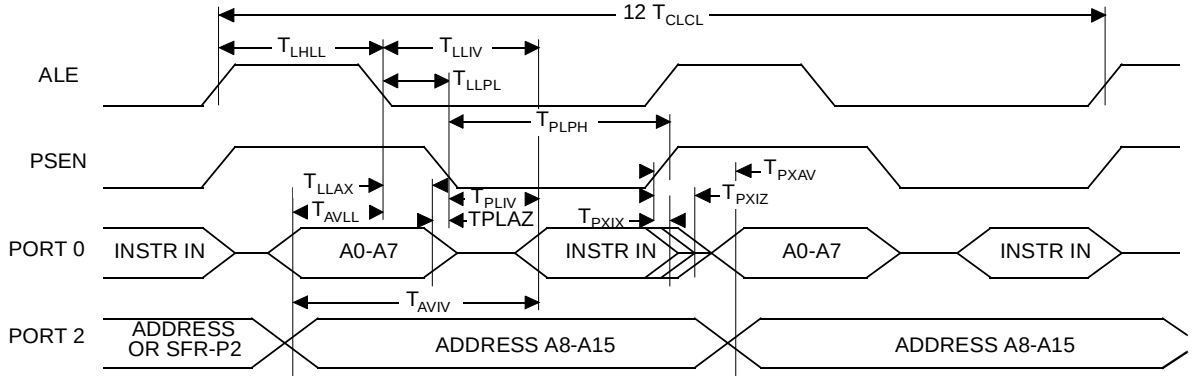
**Table 15.** AC Parameters for a Fix Clock (F = 40 MHz)

| Symbol | Min | Max | Units |
|---|---|---|---|
| T | 25 | | ns |
| $T_{LHLL}$ | 40 | | ns |
| $T_{AVLL}$ | 10 | | ns |
| $T_{LLAX}$ | 10 | | ns |
| $T_{LLIV}$ | | 70 | ns |
| $T_{LLPL}$ | 15 | | ns |
| $T_{PLPH}$ | 55 | | ns |
| $T_{PLIV}$ | | 35 | ns |
| $T_{PXIX}$ | 0 | | ns |
| $T_{PXIZ}$ | | 18 | ns |
| $T_{AVIV}$ | | 85 | ns |
| $T_{PLAZ}$ | | 10 | ns |

**Table 16.** AC Parameters for a Variable Clock

| Symbol | Type | Standard Clock | X2 Clock | X Parameter | Units |
|---|---|---|---|---|---|
| $T_{LHLL}$ | Min | 2 T - x | T - x | 10 | ns |
| $T_{AVLL}$ | Min | T - x | 0.5 T - x | 15 | ns |
| $T_{LLAX}$ | Min | T - x | 0.5 T - x | 15 | ns |
| $T_{LLIV}$ | Max | 4 T - x | 2 T - x | 30 | ns |
| $T_{LLPL}$ | Min | T - x | 0.5 T - x | 10 | ns |
| $T_{PLPH}$ | Min | 3 T - x | 1.5 T - x | 20 | ns |
| $T_{PLIV}$ | Max | 3 T - x | 1.5 T - x | 40 | ns |
| $T_{PXIX}$ | Min | x | x | 0 | ns |
| $T_{PXIZ}$ | Max | T - x | 0.5 T - x | 7 | ns |
| $T_{AVIV}$ | Max | 5 T - x | 2.5 T - x | 40 | ns |
| $T_{PLAZ}$ | Max | x | x | 10 | ns |

### External Program Memory Read Cycle




### External Data Memory Characteristics

**Table 17.** Symbol Description

| Symbol | Parameter |
|---|---|
| $T_{RLRH}$ | $\overline{RD}$ Pulse Width |
| $T_{WLWH}$ | $\overline{WR}$ Pulse Width |
| $T_{RLDV}$ | $\overline{RD}$ to Valid Data In |
| $T_{RHDX}$ | Data Hold After $\overline{RD}$ |
| $T_{RHDZ}$ | Data Float After $\overline{RD}$ |
| $T_{LLDV}$ | ALE to Valid Data In |
| $T_{AVDV}$ | Address to Valid Data In |
| $T_{LLWL}$ | ALE to $\overline{WR}$ or $\overline{RD}$ |
| $T_{AVWL}$ | Address to $\overline{WR}$ or $\overline{RD}$ |
| $T_{QVWX}$ | Data Valid to $\overline{WR}$ Transition |
| $T_{QVWH}$ | Data set-up to $\overline{WR}$ High |
| $T_{WHQX}$ | Data Hold After $\overline{WR}$ |
| $T_{RLAZ}$ | $\overline{RD}$ Low to Address Float |
| $T_{WHLH}$ | $\overline{RD}$ or $\overline{WR}$ High to ALE high |

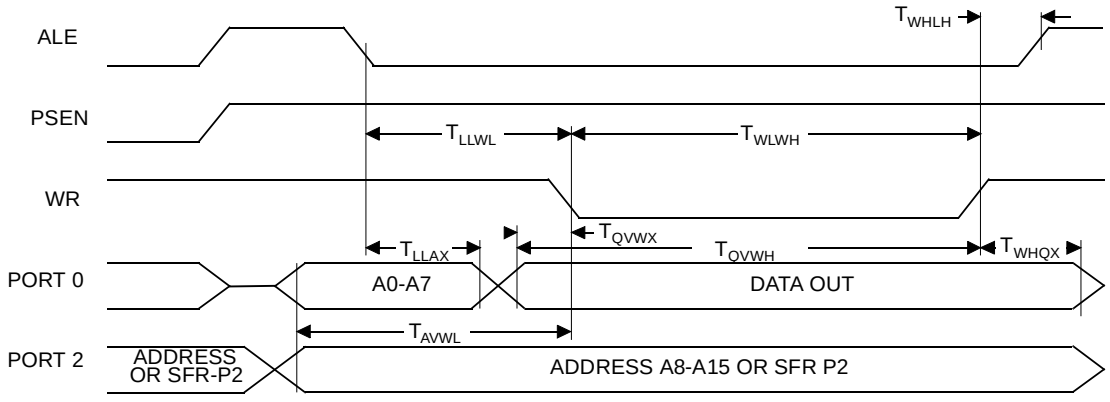
**Table 18.** AC Parameters for a Variable Clock (F = 40 MHz)

| Symbol | Min | Max | Units |
|---|---|---|---|
| $T_{RLRH}$ | 130 | | ns |
| $T_{WLWH}$ | 130 | | ns |
| $T_{RLDV}$ | | 100 | ns |
| $T_{RHDX}$ | 0 | | ns |
| $T_{RHDZ}$ | | 30 | ns |
| $T_{LLDV}$ | | 160 | ns |
| $T_{AVDV}$ | | 165 | ns |
| $T_{LLWL}$ | 50 | 100 | ns |
| $T_{AVWL}$ | 75 | | ns |
| $T_{QVWX}$ | 10 | | ns |
| $T_{QVWH}$ | 160 | | ns |
| $T_{WHQX}$ | 15 | | ns |
| $T_{RLAZ}$ | | 0 | ns |
| $T_{WHLH}$ | 10 | 40 | ns |

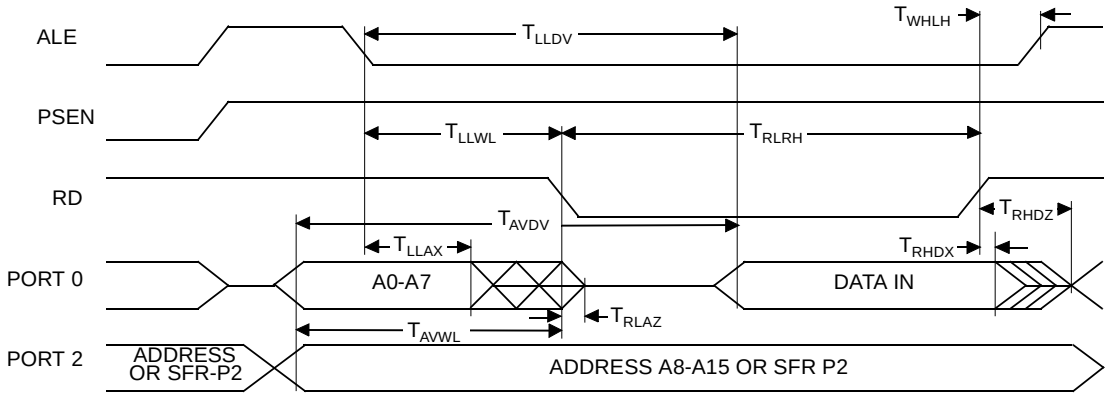
**Table 19.** AC Parameters for a Variable Clock

| Symbol | Type | Standard Clock | X2 Clock | X Parameter | Units |
|---|---|---|---|---|---|
| $T_{RLRH}$ | Min | 6 T - x | 3 T - x | 20 | ns |
| $T_{WLWH}$ | Min | 6 T - x | 3 T - x | 20 | ns |
| $T_{RLDV}$ | Max | 5 T - x | 2.5 T - x | 25 | ns |
| $T_{RHDX}$ | Min | x | x | 0 | ns |
| $T_{RHDZ}$ | Max | 2 T - x | T - x | 20 | ns |
| $T_{LLDV}$ | Max | 8 T - x | 4T -x | 40 | ns |
| $T_{AVDV}$ | Max | 9 T - x | 4.5 T - x | 60 | ns |
| $T_{LLWL}$ | Min | 3 T - x | 1.5 T - x | 25 | ns |
| $T_{LLWL}$ | Max | 3 T + x | 1.5 T + x | 25 | ns |
| $T_{AVWL}$ | Min | 4 T - x | 2 T - x | 25 | ns |
| $T_{QVWX}$ | Min | T - x | 0.5 T - x | 15 | ns |
| $T_{QVWH}$ | Min | 7 T - x | 3.5 T - x | 25 | ns |
| $T_{WHQX}$ | Min | T - x | 0.5 T - x | 10 | ns |
| $T_{RLAZ}$ | Max | x | x | 0 | ns |
| $T_{WHLH}$ | Min | T - x | 0.5 T - x | 15 | ns |
| $T_{WHLH}$ | Max | T + x | 0.5 T + x | 15 | ns |

### External Data Memory Write Cycle



### External Data Memory Read Cycle




### Serial Port Timing - Shift Register Mode

**Table 20.** Symbol Description (F = 40 MHz)

| Symbol | Parameter |
|---|---|
| $T_{XLXL}$ | Serial port clock cycle time |
| $T_{QVHX}$ | Output data set-up to clock rising edge |
| $T_{XHQX}$ | Output data hold after clock rising edge |
| $T_{XHDX}$ | Input data hold after clock rising edge |
| $T_{XHDV}$ | Clock rising edge to input data valid |

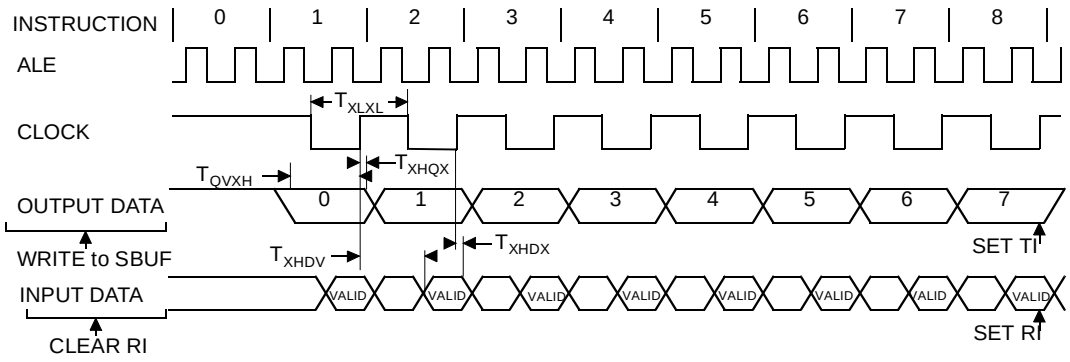
**Table 21.** AC Parameters for a Fix Clock (F = 40 MHz)

| Symbol | Min | Max | Units |
|---|---|---|---|
| $T_{XLXL}$ | 300 | | ns |
| $T_{QVHX}$ | 200 | | ns |
| $T_{XHQX}$ | 30 | | ns |
| $T_{XHDX}$ | 0 | | ns |
| $T_{XHDV}$ | | 117 | ns |

**Table 22.** AC Parameters for a Variable Clock

| Symbol | Type | Standard Clock | X2 Clock | X Parameter for -M Range | Units |
|---|---|---|---|---|---|
| $T_{XLXL}$ | Min | 12 T | 6 T | | ns |
| $T_{QVHX}$ | Min | 10 T - x | 5 T - x | 50 | ns |
| $T_{XHQX}$ | Min | 2 T - x | T - x | 20 | ns |
| $T_{XHDX}$ | Min | x | x | 0 | ns |
| $T_{XHDV}$ | Max | 10 T - x | 5 T- x | 133 | ns |

### Shift Register Timing Waveform

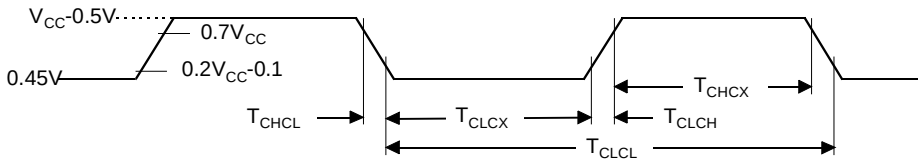



### External Clock Drive Characteristics (XTAL1)

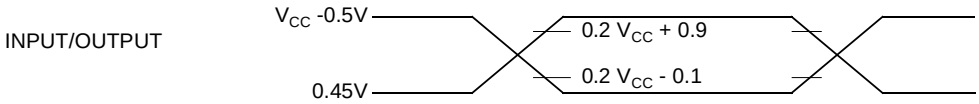
**Table 23.** AC Parameters

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{CLCL}$ | Oscillator Period | 25 | | ns |
| $T_{CHCX}$ | High Time | 5 | | ns |
| $T_{CLCX}$ | Low Time | 5 | | ns |
| $T_{CLCH}$ | Rise Time | | 5 | ns |
| $T_{CHCL}$ | Fall Time | | 5 | ns |
| $T_{CHCX}/T_{CLCX}$ | Cyclic ratio in X2 mode | 40 | 60 | % |

### External Clock Drive Waveforms

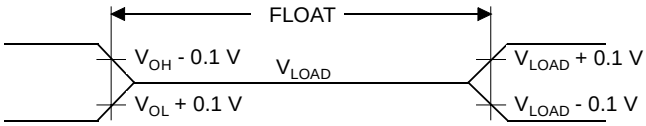



### AC Testing Input/Output Waveforms



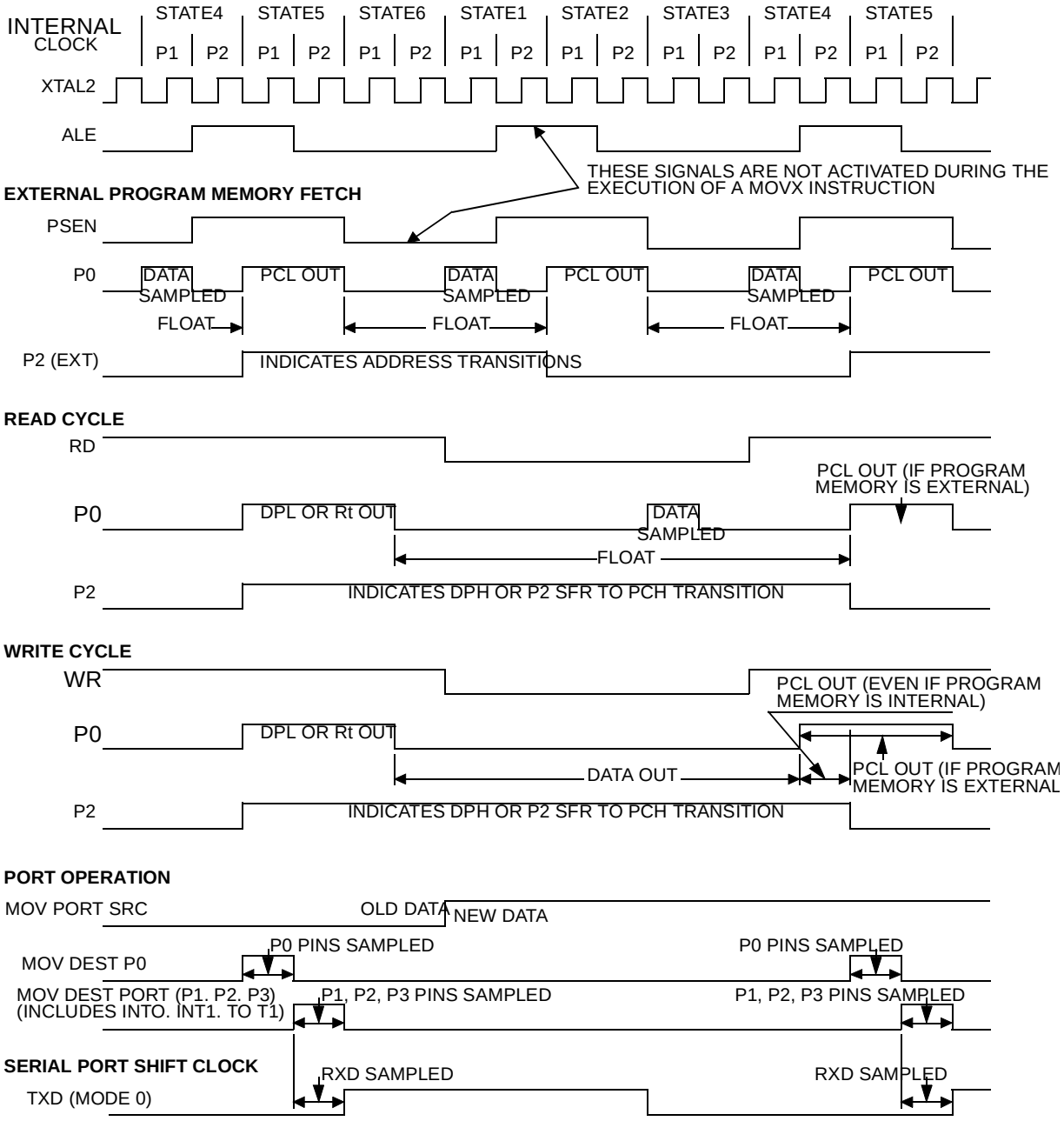

AC inputs during testing are driven at $V_{CC}$ - 0.5 for a logic “1” and 0.45V for a logic “0”. Timing measurement are made at $V_{IH}$ min for a logic “1” and $V_{IL}$ max for a logic “0”.

### Float Waveforms



For timing purposes as port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded $V_{OH}/V_{OL}$ level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

**Clock Waveforms** Valid in normal clock mode. In X2 mode XTAL2 must be changed to XTAL2/2.




This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component. Typically though ($T_A$ = 25°C fully loaded) $\overline{RD}$ and $\overline{WR}$ propagation delays are approximately 50 ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.

## Flash Memory

**Table 24.** Timing Symbol Definitions

| Signals | |
|---|---|
| S (Hardware Condition) | $\overline{PSEN}$, EA |
| R | $\overline{RST}$ |
| B | FBUSY Flag |

| Conditions | |
|---|---|
| L | Low |
| V | Valid |
| X | No Longer Valid |

**Table 25.** Memory AC Timing
VDD = 3.3V ± 10%, $T_A$ = -40 to +85°C

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{SVRL}$ | Input $\overline{PSEN}$ Valid to $\overline{RST}$ Edge | 50 | | | ns |
| $T_{RLSX}$ | Input $\overline{PSEN}$ Hold after $\overline{RST}$ Edge | 50 | | | ns |
| $T_{BHBL}$ | Flash Internal Busy (Programming) Time | | 10 | | ms |

**Figure 10.** Flash Memory - ISP Waveforms

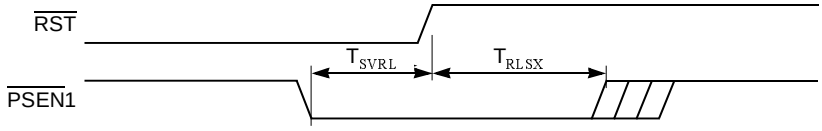
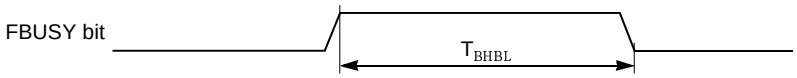



**Figure 11.** Flash Memory - Internal Busy Waveforms



## USB AC Parameters

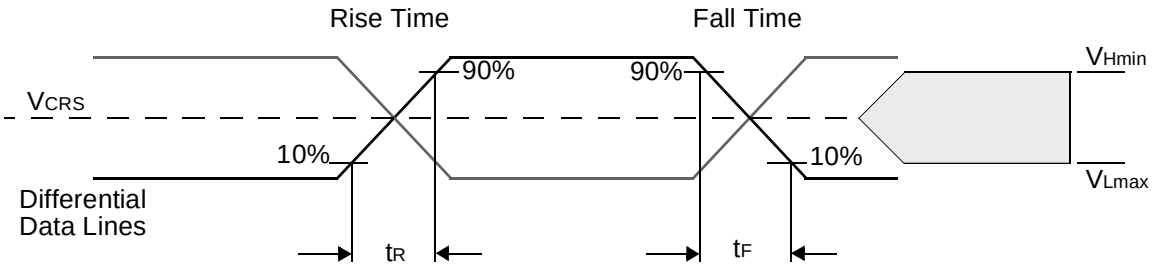



**Table 26.** USB AC Parameters

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $t_R$ | Rise Time | 4 | | 20 | ns | |
| $t_F$ | Fall Time | 4 | | 20 | ns | |
| $t_{FDRATE}$ | Full-speed Data Rate | 11.9700 | | 12.0300 | Mb/s | |
| $V_{CRS}$ | Crossover Voltage | 1.3 | | 2.0 | V | |
| $t_{DJ1}$ | Source Jitter Total to Next Transaction | -3.5 | | 3.5 | ns | |
| $t_{DJ2}$ | Source Jitter Total for Paired Transactions | -4 | | 4 | ns | |
| $t_{JR1}$ | Receiver Jitter to Next Transaction | -18.5 | | 18.5 | ns | |
| $t_{JR2}$ | Receiver Jitter for Paired Transactions | -9 | | 9 | ns | |

## Ordering Information

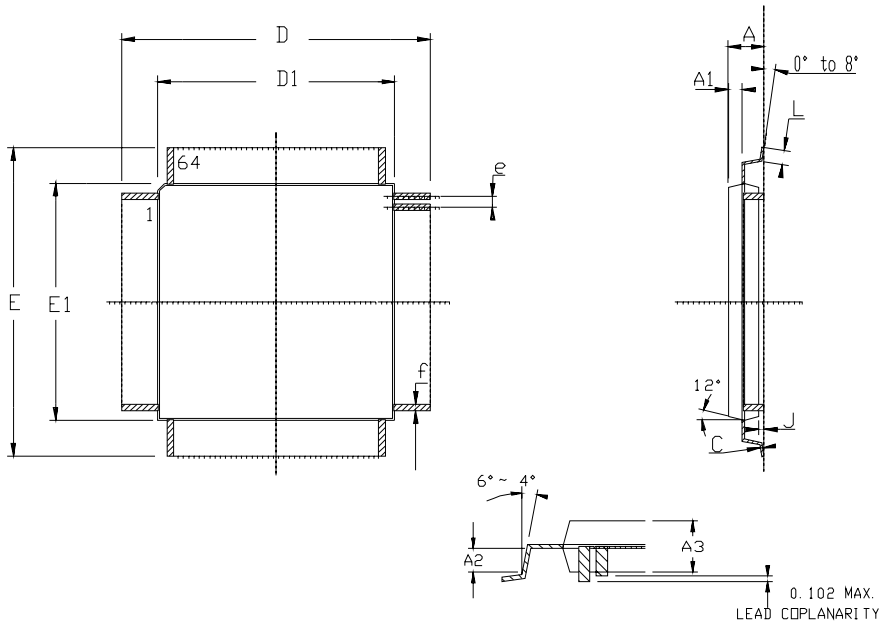
**Table 27.** Possible Order Entries

| Part Number | Memory Size (Kbytes) | Supply Voltage | Temperature Range | Package | Packing |
|---|---|---|---|---|---|
| AT89C5131A-RDTIL | 32 | 3.0 to 3.6V | Industrial | VQFP64 | Tray |
| AT89C5131A-PLTIL | 32 | 3.0 to 3.6V | Industrial | QFN48 | Stick |
| AT89C5131A-S3SIL | 32 | 3.0 to 3.6V | Industrial | PLCC52 | Stick |
| AT89C5131A-TISIL | 32 | 3.0 to 3.6V | Industrial | SO28 | Stick |

Note: 1. Optional Packing and Package options (please consult Atmel sales representative):
-Tape and Reel
-Dry Pack
-Known good dice

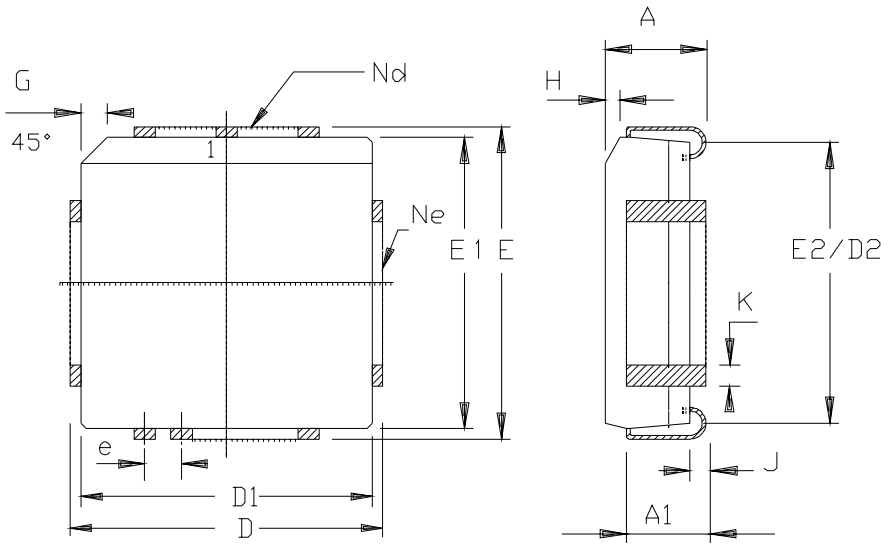
# Packaging Information

## 64-lead VQFP



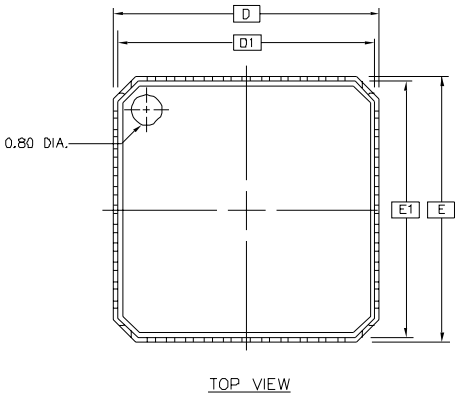

| | MM | | INCH | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | - | 1.60 | - | .063 |
| A1 | 0.64 REF | | .025 REF | |
| A2 | 0.64 REF | | .025 REF | |
| A3 | 1.35 | 1.45 | .053 | .057 |
| D | 11.75 | 12.25 | .463 | .483 |
| D1 | 9.90 | 10.10 | .390 | .398 |
| E | 11.75 | 12.25 | .463 | .483 |
| E1 | 9.90 | 10.10 | .390 | .398 |
| J | 0.05 | - | .002 | - |
| L | 0.45 | 0.75 | .018 | .030 |
| e | 0.50 BSC | | .0197 BSC | |
| f | 0.25 BSC | | .010 BSC | |

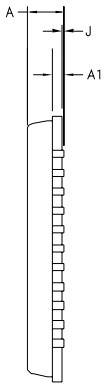
## 52-lead PLCC

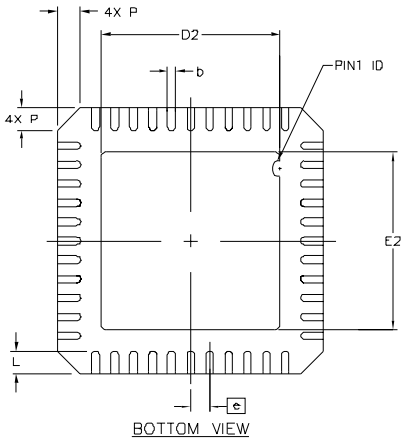



| | MM | | INCH | |
|---|---|---|---|---|
| A | 4.20 | 4.57 | .165 | .180 |
| A1 | 2.29 | 3.30 | .090 | .130 |
| D | 19.94 | 20.19 | .785 | .795 |
| D1 | 19.05 | 19.25 | .750 | .758 |
| D2 | 17.53 | 18.54 | .690 | .730 |
| E | 19.94 | 20.19 | .785 | .795 |
| E1 | 19.05 | 19.25 | .750 | .758 |
| E2 | 17.53 | 18.54 | .690 | .730 |
| e | 1.27 | BSC | .050 | BSC |
| G | 1.07 | 1.22 | .042 | .048 |
| H | 1.07 | 1.42 | .042 | .056 |
| J | 0.51 | - | .020 | - |
| K | 0.33 | 0.53 | .013 | .021 |
| Nd | 13 | | 13 | |
| Ne | 13 | | 13 | |
| PKG STD | 00 | | | |

## 48-lead MLF

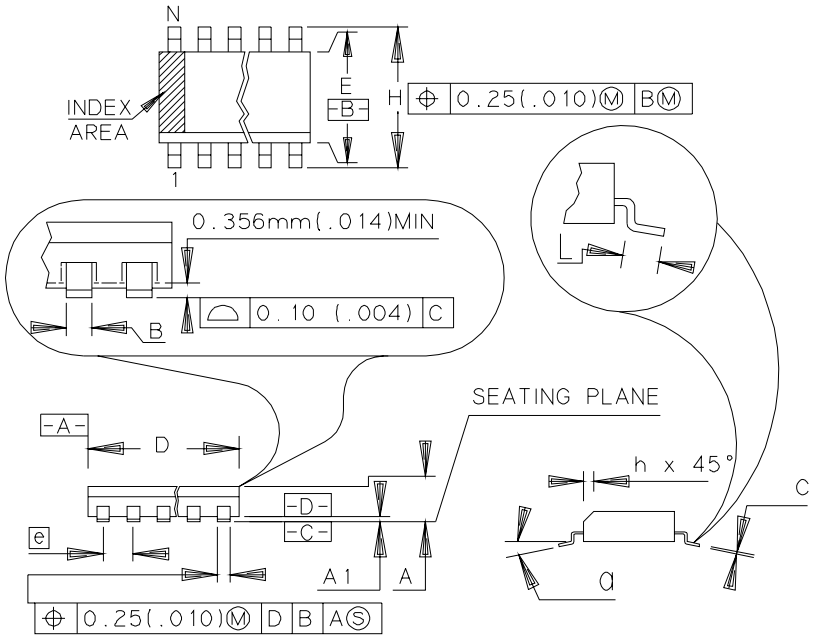



| | MM | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | – | 0.85 | 0.90 | – | .033 | .035 |
| J | 0.00 | 0.01 | 0.05 | .000 | .000 | .002 |
| A1 | | 0.20 ref | | | .008 ref | |
| D/E | | 7.00 BSC | | | .276 BSC | |
| D1/E1 | | 6.75 BSC | | | .266 BSC | |
| D2/E2 | 4.95 | 5.10 | 5.25 | .195 | .201 | .207 |
| | | | | | | |
| P | 0.24 | 0.42 | 0.60 | .009 | .016 | .024 |
| e | | 0.50 BSC | | | .020 BSC | |
| L | 0.30 | 0.40 | 0.50 | .012 | .016 | .020 |
| b | 0.18 | 0.23 | 0.30 | .007 | .009 | .012 |

## 28-lead SO




| | MM | | INCH | |
|---|---|---|---|---|
| A | 2.35 | 2.65 | .093 | .104 |
| A1 | 0.10 | 0.30 | .004 | .012 |
| B | 0.35 | 0.49 | .014 | .019 |
| C | 0.23 | 0.32 | .009 | .013 |
| D | 17.70 | 18.10 | .697 | .713 |
| E | 7.40 | 7.60 | .291 | .299 |
| e | 1.27 | BSC | .050 | BSC |
| H | 10.00 | 10.65 | .394 | .419 |
| h | 0.25 | 0.75 | .010 | .029 |
| L | 0.40 | 1.27 | .016 | .050 |
| N | 28 | | 28 | |
| a | 0° | | 8° | |

## Table of Contents

## Atmel Headquarters


***Corporate Headquarters***
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 487-2600

***Europe***
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
TEL (41) 26-426-5555
FAX (41) 26-426-5500

***Asia***
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

***Japan***
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581


## Atmel Operations


***Memory***
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

***Microcontrollers***
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
TEL (33) 2-40-18-18-18
FAX (33) 2-40-18-19-60

***ASIC/ASSP/Smart Cards***
Zone Industrielle
13106 Rousset Cedex, France
TEL (33) 4-42-53-60-00
FAX (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
TEL (44) 1355-803-000
FAX (44) 1355-242-743

***RF/Automotive***
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
TEL (49) 71-31-67-0
FAX (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

***Biometrics/Imaging/Hi-Rel MPU/ High Speed Converters/RF Data-com***
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
TEL (33) 4-76-58-30-00
FAX (33) 4-76-58-34-80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***e-mail***
literature@atmel.com

***Web Site***
http://www.atmel.com





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